In the Claims:

Please cancel claims 1-2. Please amend claims 3, 5, 7, 8, and 27. The claims are as follows:

1-2. (Canceled)

3. (Currently amended) ~~The method of claim 2, further comprising:~~ A method of testing a semiconductor chip having a plurality of common I/Os associated therewith, the method comprising the steps of:

connectivity testing a chip-to-package connection of at least one common I/O of the plurality of common I/Os, wherein the connectivity testing comprises: launching a transition through the common I/O to an associated I/O package connection and pad; and observing a response of the transition;

determining whether the chip-to-package connection is faulty from a result of the connectivity testing; and

triggering a first latch at an initialization of the transition response and triggering a second latch when the transition response has reached a transition threshold value.

4. (Original) The method of claim 3, wherein determining whether the chip-to-package connection is faulty comprises: comparing a difference between values stored in association with the first and second latches.

5. (Currently amended) ~~The method of claim 1~~ A method of testing a semiconductor chip having a plurality of common I/Os associated therewith, the method comprising the steps of:

connectivity testing a chip-to-package connection of at least one common I/O of the plurality of common I/Os; and

determining whether the chip-to-package connection is faulty from a result of the connectivity testing, wherein determining whether the chip-to-package connection is faulty comprises: comparing a first RC constant associated with a first signal relating to a connectivity testing of a first I/O with a second RC constant associated with a second signal relating to a connectivity testing of a second I/O.

6. (Original) The method of claim 5, further comprising identifying the first I/O as having a faulty connection if the first RC constant is greater than the second RC constant.

7. (Currently amended) The method of claim [[1]] 3, wherein ~~performing connectivity testing~~ launching the transition comprises generating a transition signal from a driver of the common I/O, wherein the driver is configured as a weak driver that is sensitive to capacitative loading.

8. (Currently amended) ~~The method of claim 7, wherein further comprising~~ A method of testing a semiconductor chip having a plurality of common I/Os associated therewith, the method comprising the steps of:

connectivity testing a chip-to-package connection of at least one common I/O of the plurality of common I/Os, wherein said connectivity testing comprises generating a transition

signal from a driver of the common I/O, and wherein the driver is configured as a weak driver that is sensitive to capacitative loading;

determining whether the chip-to-package connection is faulty from a result of the connectivity testing; and

placing an additional impedance into connection with the driver prior to generating the transition signal.

9. (Original) The method of claim 8, wherein placing an additional impedance into connection with the driver comprises placing a resistor into series connection with the driver.

10. (Previously presented) The method of claim 8, further comprising electrically shorting the additional impedance from connection with the driver after generating the transition signal.

11. (Original) The method of claim 10, wherein electrically shorting the additional impedance includes completing a circuit around the additional impedance to bypass the additional impedance.

12-19. (Canceled)

20. (Previously presented) The method of claim 9, wherein the resistor has an electrical resistance of at least 1 kΩ.

21. (Previously presented) The method of claim 9, wherein the resistor has an electrical resistance of at least 10 kΩ.

22. (Previously presented) The method of claim 9, wherein the resistor has an electrical resistance of at least 35 kΩ.

23. (Previously presented) The method of claim 9, wherein the resistor is electrically interposed between the driver and the common I/O.

24. (Previously presented) The method of claim 8, wherein placing an additional impedance into connection with the driver comprises placing a field effect transistor (FET) into series connection with the driver.

25. (Previously presented) The method of claim 24, wherein the FET is electrically interposed between the driver and the common I/O.

26. (Previously presented) The method of claim 8, wherein the additional impedance is electrically interposed between the driver and the common I/O.

27. (Currently amended) The method of claim 7, further comprising providing semiconductor circuitry between the driver and ~~the~~ a control ~~I/O~~ pad.

28. (Previously presented) The method of claim 27, wherein the semiconductor circuitry includes at least one of a clock tree, a latch, and a receiver.